UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,215	08/20/2003	Darel N. Emmot	10001763-1	5465

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EXAMINER
CHAUHAN, ULKA J

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/644,215	EMMOT ET AL.
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-16_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-16_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _20 August 2003_ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date 8/20/03

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2.   Claims 7-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites the limitation "the subsystem" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   **Claims 1, 2, 5-10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,951,672 to Kwok et al.**

5.   As per claim 7, Kwok teaches multiprocessor system comprising:

a host processor configured to execute a single-threaded application (Fig. 3: *system control processor 102*; c. 5 ll. 12-17: *an application program running on the system control processor 102*);

partitioning logic for partitioning the state-sequenced information, communication logic configured to communicate the partitioned state-sequenced information across a plurality of input/output busses (Fig. 4 and c. 5 ll. 51-57: *Upon receiving a graphics order to*

render a scene, graphics control processor 110b passes the graphics data associated

with the graphics order on to geometry subsystem 110c; c. 6 ll. 1-7: the geometry

subsystem 110c is implemented as a multi-threaded parallel processor; Fig. 5 and c. 9 ll.

49: blocks 16-26 correspond to the geometry subsystem 110c);

a plurality of interfaces located at the subsystem for receiving the information communicated

across the plurality of the input/output busses (Fig. 5: *input graphics work buffer 16 and*

18);

processing logic for controlling the processing of the partitioned information without re-

sequencing the information, the processing logic configured to preserve state information

of the information processed (c. 6 ll. 43-48: *the graphics control processor 110b*

supervises the operation of the graphics subsystem 110 and controls the operations

performed by the other elements of the graphics subsystem; c. 9 ll. 33-38: another set of

threads is used to grab the buffer from the queue and complete the remainder of the work

before handing the buffer to the rasterizer).

6.   As per claim 8, Kwok discloses a buffer memory in communication with the host

processor for storing state-sequenced information for communication to a subsystem (c. 9 ll. 26-

33: *the buffering thread copies the current color, texture, and surface normal coordinates as*

necessary into the vertex data structure, and stores the vertex in a buffer. The buffering thread

also flushes the vertex buffer when State Management calls, other than vertex related data, are

encountered. The buffering thread also adds this buffer to a queue of buffers for a given

context).

7.   As per claim 9, Kwok discloses that the processing logic is located at the subsystem (Fig.

4: *graphics subsystem 110 comprising graphics control processor 110b*).

8.   As per claim 10, Kwok the partitioning logic is located in at the subsystem (Fig. 4:

graphics subsystem 110 comprising graphics control processor 110b).

9.   As per claim 12, Kwok discloses that the system is a computer graphics system (Fig. 3:

graphics processing system 100).

10.   As per claim 13, Kwok discloses that the processing logic comprises at least one

geometry accelerator (Fig. 4: *geometry subsystem 110c*; Fig. 5: *geometry pipe A and geometry*

pipe B).

11.   Claims 1, 5, and 6 are similar in scope to claims 7 and 12, and are rejected under the

same rationale.

12.   As per claim 2, Kwok discloses obtaining state information from the received

information, and processing the information in a proper state context (c. 9 ll. 26-29: *the buffering*

thread copy the current color, texture, and surface normal coordinates as necessary into the

vertex data structure, and store the vertex in a buffer).

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.   /

14.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15.   Claims 3, 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent No. 5,951,672 to Kwok et al and Applicant's Admitted Prior Art (APA) [0001-

0003].

16.   As per claim 14, Kwok discloses system bus 106 but does not expressly teach that each

of the input/output busses are peripheral component interface (PCI) busses. APA disclose that

the host computer and the subsystem are coupled over an industry standard interface such as the

PCI [0003]. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have utilized an industry standard interfaces such as the PCI busses for

coupling the geometry processors in the graphics subsystem.

17.   Claim 4 is similar in scope to claim 14 and is rejected under the same rationale.

18.   As per claim 3, Kwok does not expressly teach performing at least one direct memory

access (DMA) across each of the plurality of input/output busses. APA discloses that frequently,

the communication mechanism for communicating the state-sequenced information from the host

computer 110 to the subsystem 120 includes a direct memory access (DMA) transfer [0002]. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to

have utilized DMA transfers as taught by APA in combination with receiving graphics orders in

Kwok's system in order to transfer graphics orders more quickly to the graphics subsystem

without any CPU intervention.

19.   Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent

No. 5,951,672 to Kwok et al and U.S. Patent No. 6,771,269 to Radecki et al.

20.   As per claim 11, Kwok does not expressly teach that the partitioning logic is located in at

the at the host processor. Radecki, in analogous art, teaches a video graphics system 300 in

which an application 313, being executed on a CPU 301, stores vertex information including

vertex position, normal, color, and other attributes, in vertex buffers 327 in system memory 307

or in the video card local memory 309 (Fig. 3, c. 5 ll. 51-65, c. 7 ll. 31-34, and c. 8 ll. 9-17).

Radecki discloses that in the case that the graphics processor's processing load is heavy, the

graphics driver on the CPU 301 processes vertex information in order to maintain a desired level

of system throughput (c. 11 ll. 43-67). Radecki is concerned with improving processing

throughput in the video graphics system by substantially reducing the idle time of the host

application and graphics driver particularly during periods of peak processing by the graphics

processor (c. 4 ll. 20-25) by having the CPU based graphics driver assisting in processing vertex

data (c. 11 ll. 43-67 and c. 17 ll. 4-14). Therefore, based on the desire to reduce the idle time of

the host application and graphics driver as disclosed by Radecki, it would have been obvious at

the time the invention was made, to have utilized Radecki's method in combination with Kwok's

system. Based on the knowledge commonly available to one of ordinary skill in the art, on

would have the host application allocate vertex buffers in the system memory where the video

card memory does not have sufficient space for storing additional vertex buffers in cases where

prior vertex buffers have not been processed due to the heavy load of the graphics processor.

One would have been motivated to do so in order to reduce the idle time of the application.

21.   Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent No. 5,951,672 to Kwok et al and U.S. Patent No. 6,762,763 to Migdal et al.

22.   As per claim 15, Kwok discloses that the system comprises a plurality of processing

nodes (Fig. 5: *geometry pipes A and B*; c. 1 ll. 5-10: *invention relates generally to data*

processing systems containing a plurality of data processors (i.e., multiprocessor systems) and,

in particular, to methods for synchronizing and distributing work assignments in multiprocessor

systems), but does not expressly teach that they are coupled through a communication network.

Migdal, in an analogous art, teaches a network based computer system comprising plural nodes

including a plurality of geometry subsystem nodes (Fig. 1: *G subsystems 101*). Migdal further

discloses that the network based computer system can be scaled by adding one or more G

subsystems to increase performance (c. 5 ll. 15-16 and ll. 32-34). It would have been obvious to

one of ordinary skill in the art at the time the invention was made to have utilized Migdal's

network based computer system in combination with Kwok's multiprocessor system in order to

increase the system performance by including additional geometry subsystems as taught by

Migdal.

23.   As per claim 16, Kwok discloses the processing logic comprises work queues maintained

among the processing nodes (c. 9 ll. 26-38: *The buffering thread also adds this buffer to a queue*

of buffers for a given context (or application level thread). Another set of threads is used to grab

the buffer from the queue and complete the remainder of the work, such as lighting, texturing,

conversion to NDC coordinates, etc., before handing the buffer to the rasterizer; Fig. 5: work

buffer 16 and 18).

Conclusion

24.   The following prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

US006819325B2   US006725296B2   US006384833B1   US006377257B1

   US006292200B1   US006181346B1   US005920326A   US005448698A

25.   Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The
examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.
26.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the
organization where this application or proceeding is assigned is 703-872-9306.
27.   Information regarding the status of an application may be obtained from the Patent
Application Information Retrieval (PAIR) system. Status information for published applications
may be obtained from either Private PAIR or Public PAIR. Status information for unpublished
applications is available through Private PAIR only. For more information about the PAIR
system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR
system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 17, 2005